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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MILLS, DONALD L	
ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/376,904	YASUKAWA ET AL.	
	Examiner	Art Unit	
	Donald L. Mills	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-11,27,29,35 and 41-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-11,27,29,35 and 41-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 2, 4-11, 27, 29, 35, and 41-46 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 2, 11, 27, 29, and 35, the claims specify *an actual cell* (For example, see claim 1, line 17.) The meaning of "an actual cell" is unclear from the context of the claim. It is unclear whether an "an actual cell" is, for example, a VBR or CBR cell or some other variation. Further clarification is requested.

Regarding claims 1, 2, 11, 27, 29, and 35, the claims specify *a dummy cell* (For example, see claim 1, line 18.) The meaning of "a dummy cell" is unclear from the context of the claim. Typically the prior art refers to "idle cells" as cells which contain no data. Further clarification is requested.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4, 5, 11, 27, 29, and 35 rejected under 35 U.S.C. 103(a) as being unpatentable over Aramaki (US 5,485,457) in view of Fan (US 5,337,308).

Regarding claims 1, 2, 11, 27, 29 and 35, Aramaki discloses a packet (ATM) switching system capable of reducing a delay time for each packet, which comprises:

At least one basic switch, said basic switch including means for referring to time information written in a header of an input cell and for switching cells to an output port in an ascending order of said time information, said means including (Referring to Figure 9, tertiary switch **25**, read time stamps (header) assigned to packets for switching cells to an output in ascending order of time stamp. See column 14, lines 15-29.)

Plural cross-points, wherein at each of the cross-points an input line and an output line are crossed, and wherein the plural cross-points are layered, each cross-point including (Referring to Figure 9, tertiary switch **25** comprises plural cross-points between plural, layered input lines and output lines.)

A first buffer which stores the extracted cell (Referring to Figure 9, FIFO **38-1** stores the sensed (extracted) packet. See column 13, lines 50-55;)

A second buffer which stores a cell arriving from another cross-point (Referring to Figure 9, FIFO **38-2** stores the sensed packet arriving from another switch. See column 13, lines 50-55;)

Means for comparing time information of a head cell in said first buffer with time information of a head cell in said second buffer and for sending a head cell with earlier time information to the another cross-point or said output port (Referring to Figure 9, memory output control circuit **42** receives time-stamps

(head cell) assigned to packets from alignment memories **38-1** to **38-8** and selects the earliest inputted time stamps (comparison of head cell in first and second buffer). See column 14, lines 18-23.)

Aramaki further teaches *a first stage* and *a second stage* (Referring to Figure 3, primary switch **23** and secondary switch **24**.)

Aramaki does not expressly disclose *an address filter for extracting a cell arriving from the input line.*

The Examiner interprets the address filter as the time-stamp filter. Aramaki is silent with regards to extracting time stamps. However, Aramaki teaches receiving packets arriving from input lines and comparing time stamps of arriving packets for determining the proper output order.

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement an address filter (time stamp filter) in the system of Aramaki. One of ordinary skill in the art at the time of the invention would have been motivated to do so in order to compare the time stamps of Aramaki in a straight-forward and efficient manner as taught by Aramaki (See column 2, lines 38-40.)

Aramaki does not disclose *wherein said address filter captures a cell having an address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell or said dummy cell in said first buffer.*

Fan teaches a low delay ATM switching system using idle cells stamped with reference time in a multi-stage switching system. A time stamp is attached to each cell at an entry point of

the system indicating the arrival of the cell, and the cell is transferred to a network comprising multiple switching stages each being composed of basic switching modules. The time stamp of cells arriving at a given one of the switching modules, where the cells are likely to arrive out of sequence, is constantly monitored and a minimum value of the time stamps is detected and buffered. When an empty buffer exists in the given switching module, and idle cell containing the time stamp of the minimum value is generated at the output of the empty buffer (See Figure 2 and Abstract.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the idle cells of Fan in the system of Aramaki. One of ordinary skill in the art at the time of the invention would have been motivated to do so in order to avoid congestion of cells destined to particular routes as taught by Fan (See column 4, lines 63-65.)

Regarding claim 4, the primary reference further discloses *wherein input lines connected to the cross-points are classified into a plurality of groups* (Referring to Figures 3 and 9, inputs to FIFO's **38-1** to **38-8** for each tertiary switch **25**;) *Said first buffer storing cells arriving from said input lines of one of said groups* (Referring to Figures 3 and 9, FIFO **38-1** receives a packet that arrives from its corresponding input;) *Time information of a cell with the earliest time information among cells in said first buffer being compared with time information of said head cell in said second buffer, and a cell with earlier time information being sent to a cross-point or said output port* (Referring to Figure 9, memory output control circuit **42** receives time-stamps assigned to packets from alignment memories **38-1** to **38-8** and selects the earliest inputted time stamps (comparison of head cell in first and second buffer). See column 14, lines 18-23.)

Regarding claim 5, the primary reference further teaches *further comprising adding*

means which adds arriving time information to an arriving cell as said time information (Referring to Figures 3 and 9, tertiary switch **25**, read time stamps assigned to packets by the time stampers **22**. See column 14, lines 15-29.)

Regarding claim 6 as explained in the rejection of claim 1, the primary reference teaches all of the claim limitations of claim 1 (parent claim).

Aramaki does not disclose *wherein said adding means generates a dummy cell and adds time information to said dummy cell if there is no input.*

Fan teaches a low delay ATM switching system, which comprises a RT cell generator that can be considered as part of the "adding means" of the Fan system. The RT cell generator creates idle cells with time stamps when there is an empty buffer detected (See Figure 3 and column 6, lines 41-58.)

It would have been obvious to one ordinary skill in the art at the time of the invention to implement the idle cell generator of Fan in the system of Aramaki. One of ordinary skill in the art at the time of the invention would have been motivated to do so in reduce unnecessary delay due to buffer underflow.

Regarding claim 7 as explained in the rejection of claim 1, the primary reference teaches all of the claim limitations of claim 1 (parent claim).

Aramaki does not disclose *wherein said basic switch transfers said dummy cells or said arriving cells with said time information to output ports other than the destination of said arriving cell.*

Fan teaches the transferring of idle cells to the next stage of the switch over an output line (See Figure 3.)

It would have been obvious to one ordinary skill in the art at the time of the invention to implement the idle cell generator of Fan in the system of Aramaki. One of ordinary skill in the art at the time of the invention would have been motivated to do so in reduce unnecessary delay due to buffer underflow.

Regarding claim 8 as explained in the rejection of claim 1, the primary reference teaches all of the claim limitations of claim 1 (parent claim).

Aramaki does not disclose *wherein said basic switch allows said dummy cell to be overwritten by an arriving cell.*

Fan teaches that idle cells can be overwritten (See column 6.)

It would have been obvious to one ordinary skill in the art at the time of the invention to implement the idle cell generator of Fan in the system of Aramaki. One of ordinary skill in the art at the time of the invention would have been motivated to do so in reduce unnecessary delay due to buffer underflow.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aramaki (US 5,485,457), in view of Fan, further in view of Averbuch et al. (US 6,160,805), hereinafter referred to as Averbuch.

Regarding claim 9 as explained in the rejection of claim 1, the primary reference teaches all of the claim limitations of claim 1 (parent claim). Aramaki further discloses *wherein said time information is a value repeating periodically* (inherently, the time must repeat since there is only a certain number of bits used for the time in the header of the cell.)

Aramaki does not disclose *said adding means adding a flag for identifying said period to said cell, and said basic switch identifying said period by referring to said flag.*

Averbuch discloses a system wherein Beginning of Transmission (BOT) and End of Transmission (EOT) flags are used to indicate a transmission time period for a cell (See column 5, lines 36-50.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the marking system of Averbuch in the system of Aramaki. One of ordinary skill in the art would have been motivated to do so in order to ensure fair usage of the switching resources since each cell is given only a particular time period for transmission.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aramaki (US 5,485,457), in view of Fan, further in view of Henrion (US 5,127,000).

Regarding claim 10 as explained in the rejection of claim 1, the primary reference teaches all of the claim limitations of claim 1 (parent claim).

Aramaki does not disclose *wherein said basic switch includes a delay time counter, adds said delay time, and uses said added delay time as said time information.*

Henrion teaches a system wherein a delay time for each cell is entreated into the header field of the cell (See Figures 5 and 6, column 6, lines 29-40 and claim 8.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the delay tracking of Henrion in the system of Aramaki. One of ordinary skill in the art at the time of the invention would have been motivated to do so in order to process cells

depending on the delay, thereby making sure the cells experiencing the longest delay are processed first to help ensure quality of service of the system.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 2, 4-11, 27, 29 and 35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donald L. Mills whose telephone number is 571-272-3094. The examiner can normally be reached on 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donald L Mills
DLM
January 6, 2006

JOHN PEZZLO
PRIMARY EXAMINER